

## Claims

We claim:

- 1           1.       A heterojunction bipolar transistor (HBT), comprising:  
2           a collector formed over a substrate;  
3           a base formed over the collector;  
4           an emitter formed over the base; and  
5           a tunneling suppression layer between the collector and the base, the tunneling  
6           suppression layer fabricated from a material that is different from a material of the base  
7           and that has an electron affinity equal to or greater than an electron affinity of the  
8           material of the base.
- 1           2.       The HBT of claim 1, in which the collector comprises indium phosphide,  
2           the base comprises gallium arsenide antimonide, the emitter comprises two or more of  
3           indium, phosphorous, aluminum, gallium, nitrogen and arsenic, and the tunneling  
4           suppression layer is a material comprising two or more of aluminum, gallium, indium,  
5           nitrogen, phosphorous, arsenic and antimony.
- 1           3.       The HBT of claim 2, in which the tunneling suppression layer comprises  
2           aluminum gallium indium arsenide.
- 1           4.       The HBT of claim 3, in which the tunneling suppression layer comprises  
2            $\text{Al}_{0.33}\text{Ga}_{0.15}\text{In}_{0.52}\text{As}$ .
- 1           5.       The HBT of claim 3, in which the tunneling suppression layer consists  
2           essentially of  $\text{Al}_{1-x-y}\text{Ga}_x\text{In}_y\text{As}$ , where  $0.09 \leq x \leq 0.25$ , and  $y=0.52$ .
- 1           6.       The HBT of claim 3, in which the tunneling suppression layer is structured  
2           to provide a graded electron affinity,  $\chi$ .

1           7.     The HBT of claim 6, in which the tunneling suppression layer consists  
2 essentially of  $\text{Al}_{1-x-y}\text{Ga}_x\text{In}_y\text{As}$ , where  $0.09 \leq x \leq 0.25$ , and  $y=0.52$  and has a greater gallium  
3 mole-fraction near the collector than near the base.

1           8.     The HBT of claim 2, in which the tunneling suppression layer comprises  
2 aluminum indium arsenide phosphide.

          9.     The HBT of claim 8, in which the tunneling suppression layer comprises  
indium phosphide and aluminum indium arsenide having between 40% and 100% indium  
phosphide.

1           10.    The HBT of claim 9, in which the tunneling suppression layer comprises  
2 indium phosphide and aluminum indium arsenide having 58% indium phosphide and  
3 42% aluminum indium arsenide near the base and 75% indium phosphide and 25%  
4 aluminum indium arsenide near the collector.

1           11.    The HBT of claim 2, in which the tunneling suppression layer is formed of  
2 a digital alloy composite comprising aluminum gallium indium arsenide.

1           12.    The HBT of claim 11, in which the digital alloy composite comprises  
2  $\text{Al}_{0.33}\text{Ga}_{0.15}\text{In}_{0.52}\text{As}$ , using alternating layers of  $\text{Al}_{0.48}\text{In}_{0.52}\text{As}$  and  $\text{Ga}_{0.47}\text{In}_{0.53}$ .

1           13.    A method of making a heterojunction bipolar transistor, the method  
2 comprising:  
3           providing a substrate;  
4           forming a subcollector over the substrate;  
5           forming a collector over the subcollector;  
6           forming a tunneling suppression layer over the collector;

7           forming a base over the tunneling suppression layer; and  
8           forming an emitter over the base,  
9           wherein the tunneling suppression layer is formed using a material that is different  
10          from a material of the base and that has an electron affinity equal to or greater than an  
11          electron affinity of the material of the base.

1           14.     The method of claim 13, further comprising forming the collector using  
2          indium phosphide, forming the base using gallium arsenide antimonide, forming the  
3          emitter using a material comprising two or more of indium, phosphorous, aluminum,  
4          gallium, nitrogen and arsenic, and forming the tunneling suppression layer using a  
5          material comprising two or more of aluminum, gallium, indium, nitrogen, phosphorous,  
6          arsenic and antimony.

1           15.     The method of claim 14, further comprising forming the tunneling  
2          suppression layer using aluminum gallium indium arsenide.

1           16.     The method of claim 15, in which the tunneling suppression layer  
2          comprises  $\text{Al}_{0.33}\text{Ga}_{0.15}\text{In}_{0.52}\text{As}$ .

1           17.     The method of claim 15, in which the tunneling suppression layer consists  
2          essentially of  $\text{Al}_{1-x-y}\text{Ga}_x\text{In}_y\text{As}$ , where  $0.09 \leq x \leq 0.25$ , and  $y=0.52$ .

1           18.     The method of claim 15, in which forming the tunneling suppression layer  
2          comprises forming the tunneling suppression layer with a graded electron affinity,  $\chi$ .

1           19.     The method of claim 18, further comprising forming the tunneling  
2          suppression layer essentially of  $\text{Al}_{1-x-y}\text{Ga}_x\text{In}_y\text{As}$ , where  $0.09 \leq x \leq 0.25$ , and  $y=0.52$  and  
3          having greater a gallium mole-fraction near the collector than near the base.

1           20.     The method of claim 14, further comprising forming the tunneling  
2          suppression layer using aluminum indium arsenide phosphide.

1           21.    The method of claim 20, further comprising forming the tunneling  
2 suppression layer using indium phosphide and aluminum indium arsenide having 40% to  
3 100% indium phosphide.

1           22.    The method of claim 21, in which the tunneling suppression layer  
2 comprises indium phosphide and aluminum indium arsenide having 58% indium  
3 phosphide and 42% aluminum indium arsenide near the base and 75% indium phosphide  
4 and 25% aluminum indium arsenide near the collector.

1           23.    The method of claim 14, further comprising forming the tunneling  
2 suppression layer using a digital alloy composite comprising aluminum gallium indium  
3 arsenide.

1           24.    The method of claim 23, further comprising forming the digital alloy  
2 composite using alternating layers of  $\text{Al}_{0.48}\text{In}_{0.52}\text{As}$  and  $\text{Ga}_{0.47}\text{In}_{0.53}$ .

1           25.    A tunneling suppression layer, comprising two or more of aluminum,  
2 gallium, indium, nitrogen, phosphorous, arsenic and antimony.

1           26.    The tunneling suppression layer of claim 25, comprising  
2  $\text{Al}_{0.33}\text{Ga}_{0.15}\text{In}_{0.52}\text{As}$ .